Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.098”**

**.062”**

**7 6**

**2 3 4**

**811**

**MASK**

**REF**

**PAD FUNCTIONS:**

1. **NC**
2. **– IN**
3. **+ IN**
4. **–VS**
5. **NC**
6. **OUTPUT**
7. **+ VS**
8. **NC**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Floating**

**Mask Ref: 811**

**APPROVED BY: DK DIE SIZE .062” X .098” DATE: 10/25/18**

**MFG: ANALOG DEVICES THICKNESS .019” P/N: AD811S**

**DG 10.1.2**

#### Rev B, 7/19/02